Express Mail Label No.: EV 292 459 643 US
Date of Deposit: February 25, 2004
10/786, 357

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FORM P1	TO-1449/A and I	3 (Modified)	APPLICATION NO.:	Not Yet Assigned	ATTY. DOCKET NO.: A0312.70521US00	
		N DISCLOSURE	FILING DATE:	Horowatt 2/25/01	CONFIRMATION NO.: Not Yet Assigned	
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**U.S. PATENT DOCUMENTS** 

Examiner's	Cite	U.S. Patent Document		Name of Patentce or Applicant of Cited		Date of Publication or of issue	
Initials	No.	Number	Kind Code	Document		of Cited Document MM-DD-YYYY	
LN	Al	6,650,168	Bl	Wang et al.	327/333	11/18/2003	
ln	A2	6,556,061	Bl	Chen et al.	327/333	04/29/2003	
W,	A3	6,489,828	Bi	Wang et al.	327/333	12/03/2002	
en	A4	6,414,534	BI	Wang et al.	327/333	07/02/2002	
					•		

FOREIGN PATENT DOCUMENTS

Examiner's Initials	Cite No.	Foreign Patent Document			Name of Patentee or Applicant of Cited	Date of Publication of	Translation
		Office/ Country	Number		Document (not necessary)	Cited Document MM-DD-YYYY	(Y/N)
			<u>····</u>				
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OTHER ART — NON PATENT LITERATURE DOCUMENTS

Examiner's Initials	Cite No	Include name of the author (in CAPITAL LETTERS) title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, relevant page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)
LN	CI	Wen-Tai Wang et al., "Level Shifters for High-Speed 1-V to 3.3 V Interfaces in a 0/13-µm Cu- Interconnection/Low-k CMOS Technology; pp. 307-310, 2001 IEEE;	
w	C2	Texas Instruments Translation Overview; pp. 1-4, 2003;	
LN	C3	"Voltage Level Translating Circuit", Oct. 1959, IBM Technical Disclosure Bulletin;	
LN	C4	"Voltage Level Translation Circuit:, June 1975, pp. 1-2, IBM Technical Disclosure Bulletin;	
LN	C5	Charles D. Rakes, "Circuit Circus", pp. 59-62; March 1999, Popular Electronics;	
in	C6	"Cascaded Common-Gate FET IC Provides Flexible Level Translation:, Electronic Design, pp. 1 of 5; 2/3/04	

EXAMINER Long nguyen	DATE CONSIDERED 10/14/05
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